AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. - 15. (Canceled)

16. (Previously presented) A method of fabricating a self-aligned conductive region to active region structure comprising:

providing a semiconductor region within a substrate extending to a surface, forming a gate insulator layer over said semiconductor region;

forming, sequentially, a conductive layer, an insulator layer and a hard mask layer over said gate insulator layer;

patterning said gate insulator layer, said conductive layer, said insulator layer and said hard mask layer to form a plurality of tiered parallel stripes;

forming a spacer insulator layer over the sidewalls of said parallel stripes;

forming trenches in said semiconductor region between said parallel stripes;

growing an insulator liner layer over sides of said trenches and underlying said spacer insulator, and depositing an insulator filler layer so that said trenches and the space between said parallel stripes are filled with said insulator filler layer;

planarizing so that said insulator filler layer above top of said insulator layer is removed and said hard mask is removed;

etching said filler layer so that it just fills said trenches;

removing said insulator layer and said insulator spacer layer;

patterning said conductive layer to form separated conductive regions.

17. (Previously presented) The method of claim 16 wherein said semiconductor region is a silicon region.

18. (Previously presented) The method of claim 16 wherein said substrate is a silicon substrate.

19. (Previously presented) The method of claim 16 wherein said gate insulator regions are oxide regions.

20. (Previously presented) The method of claim 16 wherein said insulator liner layer is a grown oxide layer.

21. (Previously presented) The method of claim 16 wherein said insulator filler layer is an HDP oxide layer.

22. (Previously presented) The method of claim 16 wherein said conductive layer is composed of doped polysilicon.

23. (original) The method of claim 16 wherein said insulator layer is a nitride layer.

24. (original) The method of claim 16 wherein said hard mask layer is an oxide layer.

25. (original) The method of claim 16 wherein said insulator spacer layer is a nitride layer.

26. (original) The method of claim 16 wherein said planarizing is performed using CMP.

27. (Previously presented) The method of claim 16 wherein said conductive regions are gates of semiconductor integrated circuit devices.

28. (Previously presented) A method of fabricating a self-aligned floating gate to active region structure comprising:

providing a semiconductor region within a substrate extending to a surface,

forming a gate insulator layer over said semiconductor region;

forming, sequentially, a conductive layer, an insulator layer and a hard mask layer over said gate insulator layer;

patterning said gate insulator layer, said conductive layer, said insulator layer and said hard mask layer to form a plurality of tiered parallel stripes;

forming a spacer insulator layer over the sidewalls of said parallel stripes;

forming trenches in said semiconductor region between said parallel stripes;

growing an insulator liner layer over sides of said trenches and underlying said spacer insulator, and depositing an insulator filler layer so that said trenches and the space between said parallel stripes are filled with said insulator filler layer;

planarizing so that said insulator filler layer above top of said insulator layer is removed and said hard mask is removed;

etching said filler layer so that it just fills said trenches;

removing said insulator layer and said insulator spacer layer;

patterning said conductive layer to form separated floating gates.

29. (Previously presented) The method of claim 28 wherein said semiconductor region is a silicon region.

30. (Previously presented) The method of claim 28 wherein said substrate is a silicon substrate.

31. (Previously presented) The method of claim 28 wherein said gate insulator regions are oxide regions.

32. (Previously presented) The method of claim 28 wherein said insulator liner layer is a grown oxide layer.

33. (Previously presented) The method of claim 28 wherein said insulator filler layer is an HDP oxide layer.

34. (Previously presented) The method of claim 28 wherein said conductive layer is composed of doped polysilicon.

35. (original) The method of claim 28 wherein said insulator layer is a nitride layer.

36. (original) The method of claim 28 wherein said hard mask layer is an oxide layer.

37. (original) The method of claim 28 wherein said insulator spacer layer is a nitride layer.

38. (original) The method of claim 28 wherein said planarizing is performed using CMP.

39. (Previously presented) A method of fabricating a self-aligned conductive region to active region structure comprising:

providing a semiconductor region within a substrate extending to a surface,

forming a gate insulator layer over said semiconductor region;

forming, sequentially, a conductive layer and an insulator layer over said gate insulator layer;

patterning said gate insulator layer, said conductive layer and said insulator layer to form a plurality of tiered parallel stripes;

forming a spacer insulator layer over the sidewalls of said parallel stripes;

forming trenches in said semiconductor region between said parallel stripes;

growing an insulator liner layer over sides of said trenches and underlying said spacer insulator, and depositing an insulator filler layer so that said trenches and the space between said parallel stripes are filled with said insulator filler layer;

planarizing so that said insulator filler layer above top of said insulator layer is removed;

etching said filler layer so that it just fills said trenches;

removing said insulator layer and said insulator spacer layer;

patterning said conductive layer to form separated conductive regions.

40. (Previously presented) The method of claim 39 wherein said semiconductor region is a silicon region.

41. (Previously presented) The method of claim 39 wherein said substrate is a silicon substrate.

42. (Previously presented) The method of claim 39 wherein said gate insulator regions are oxide regions.

43. (Previously presented) The method of claim 39 wherein said insulator liner layer is a grown oxide layer.

44. (Previously presented) The method of claim 39 wherein said insulator filler layer is an HDP oxide layer.

45. (Previously presented) The method of claim 39 wherein said conductive layer is composed of doped polysilicon.

46. (original) The method of claim 39 wherein said insulator layer is a nitride layer.

47. (original) The method of claim 39 wherein said insulator spacer layer is a nitride layer.

48. (original) The method of claim 39 wherein said planarizing is performed using CMP.

49. (Previously presented) The method of claim 39 wherein said conductive regions are gates of semiconductor integrated circuit devices.

50. (Previously presented) A method of fabricating a self-aligned floating gate to active region structure comprising:

providing a semiconductor region within a substrate extending to a surface,

forming a gate insulator layer over said semiconductor region;

forming, sequentially, a conductive layer and an insulator layer over said gate insulator layer;

patterning said gate insulator layer, said conductive layer and said insulator layer to form a plurality of tiered parallel stripes;

forming a spacer insulator layer over the sidewalls of said parallel stripes;

forming trenches in said semiconductor region between said parallel stripes;

growing an insulator liner layer over sides of said trenches and underlying said spacer insulator, and depositing an insulator filler layer so that said trenches and the space between said parallel stripes are filled with said insulator filler layer;

planarizing so that said insulator filler layer above top of said insulator layer is removed;

etching said filler layer so that it just fills said trenches;

removing said insulator layer and said insulator spacer layer;

patterning said conductive layer to form separated floating gates.

51. (currently amended) The ~~structure~~ method of claim 50 wherein said semiconductor region is a silicon region.

52. (Previously presented) The method of claim 50 wherein said substrate is a silicon substrate.

53. (Previously presented) The method of claim 50 wherein said gate insulator regions are oxide regions.

54. (Previously presented) The method of claim 50 wherein said insulator liner layer is a grown oxide layer.

55. (Previously presented) The method of claim 50 wherein said insulator filler layer is an HDP oxide layer.

56. (Previously presented) The method of claim 50 wherein said floating gates are composed of doped polysilicon.

57. (original) The method of claim 50 wherein said insulator layer is a nitride layer.

58. (original) The method of claim 50 wherein said insulator spacer layer is a nitride layer.

59. (original) The method of claim 50 wherein said planarizing is performed using CMP.

60. (Previously presented) The method of claim 16 wherein said spacer insulator layer is on said insulator liner layer.

61. (Previously presented) The method of claim 28 wherein said spacer insulator layer is on said insulator liner layer.

62. (Previously presented) The method of claim 39 wherein said spacer insulator layer is on said insulator liner layer.

63. (Previously presented) The method of claim 50 wherein said spacer insulator layer is on said insulator liner layer.